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(54) Circuit board with primary and secondary through holes

(57) A circuit board is provided which has contacts on the surface arrayed to engage contact pads on a chip carrier bounded by a grid. A plurality of primary through holes are provided in the circuit board location within the grid in an interstitial array and electrically connected to respective first chip contact pads thereabove. A plurality of secondary through holes are provided which are located outside the grid and electrically connected to respective second chip contact pads.

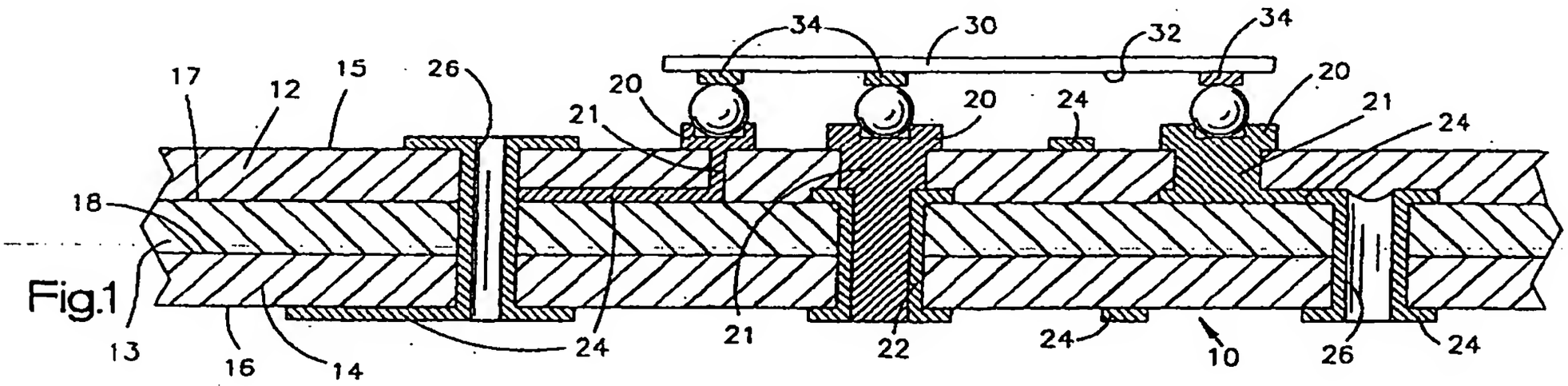

Fig.1

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Description

The present invention relates to an improved multi-layer printed circuit board capable of achieving a high degree of wiring density.

As modern chip carriers become more compact, it becomes ever more difficult to connect the carriers to underlying circuit boards without shorting between adjacent electrical contacts. Accordingly, it is desirable to develop a new design for circuit boards which will allow even greater wiring density than possible in the past.

According to one aspect of the present invention there is provided a multi-layer circuit board for receiving a chip carrier having a high density array of electrical contact pads arranged in a grid, said circuit board comprising

an electrically insulating substrate having upper and lower surfaces,
a plurality of electrical contacts on said upper surface for connection to the electrical contact pads of said chip carrier,
a first wiring layer having electrical contacts therein,
a second wiring layer having wiring traces therein,
said second wiring layer being associated with the upper surface of said substrate,
wherein said circuit board has primary through holes arranged within said grid in an interstitial array and secondary through holes located outside said grid, said primary through holes being in electrical communication with respective first electrical contacts of said upper surface,
respective second electrical contacts on said upper surfaces being in electrical contact with said second through holes.

In accordance with the present embodiment, a novel multi-layer circuit board is provided. This circuit board includes primary through holes arranged within the grid defined by the electrical contact pads of the chip carrier, these primary through holes being arranged in an interstitial array corresponding to a subset of the contact pads on the chip carrier. Those contact pads on the carrier not connected to one of these primary through holes are connected to secondary through holes arranged outside the chip carrier grid.

Connecting only some of the chip carrier contact pads to through holes within the grid defined by the chip carrier opens the spacing between adjacent through holes in this area, thereby allowing more traces and wider trace widths, spaces and land sizes to be accommodated in these areas between adjacent through holes. This, in turn, facilitates higher wiring density and flexibility. Connecting the remaining chip carrier contact pads to through holes located outside the chip carrier grid allows denser arrays on the chip carrier, thereby contributing to compactness. As a result, through the use of blind vias, wiring density and flexibility are significantly improved, while overall device compactness is still maintained.

The present invention may be more readily understood by reference to the following drawings wherein:

Fig. 1 is a schematic longitudinal section illustration of a portion of a multi-layer circuit board made in accordance with the present invention, the circuit board having mounted thereon a high density chip carrier;
Fig. 2 is a view similar to Figure 1 but showing additional layers of dielectric material and circuitry in accordance with this invention;
Fig. 3 is a schematic illustration of the array of electrical contact pads on the circuit board to mate with the contacts on a chip carrier;
Fig. 4 is a schematic internal plan view illustrating the array of primary through holes in the circuit board of Fig. 1 which are located within the grid defined by the chip carrier of Fig 1; and
Fig. 5 is a schematic internal plan view similar to Fig. 3 showing the through holes located both inside and outside the interstitial grid.

Referring to Fig. 1, a novel multi-layer circuit board in accordance with the present invention, generally indicated at 10, is composed of three layers 12, 13 and 14 of electrical insulating material such as FR4, a glass reinforced epoxy. The layer 12 has an upper surface 15, the layer 14 has a lower surface 16, and two intermediate internal surfaces 17 and 18 are defined between layers 12/13 and 13/14, respectively. In addition, circuit board 10 includes a plurality of contacts 20 on the surface 15 of the substrate. These contacts 20 are arranged in the pattern of the contacts on the I/C chip carrier to be attached, which will be referred to hereinafter sometimes as the grid. Some of the contacts 20 are connected by blind vias 21 to filled plated through holes 22 directly therebeneath. These holes 22 may terminate at surface 18, or, as shown in Figure 1, may continue through to surface 16. These holes 22 are sometimes referred to as the primary holes. Others of the contacts 20 are connected by vias 21 to wiring 24 on surface 17 or 18 which, in turn, is connected to plated through holes 26, which can extend entirely through the substrate or extend from any surface 15, 16, 17 or 18 to any other surface. Moreover, wiring traces 24 can be provided on any of the surfaces 15, 16, 17 and 18 to interconnect holes 22, or 26 or vias 21 or pads 20. The spacing of the holes 22 and 26 allows for this wiring as will be explained presently. As will be explained in more detail presently, the plated through holes 22 are located within the grid pattern of the chip carrier, and the plated through holes 26 are located outside the grid pattern. As shown in Fig. 2, element 13 may be comprised of multiple layers of dielectric material and have multiple wiring layers 24 within it that communicate with plated through holes 22 and 26. Contacts 27 on the lower surface 16 are pro-

vided to allow solder balls 28 to connect the circuit board 10 to pads 29 on components (not shown). (Similar connections are made with the embodiment of Fig. 1.) This allows for a high density chip carrier to be connected to a substrate surface, and the electrical connections extend from plated through holes spread out beyond interstitial grid pattern allowing more room for wiring on the surfaces 15 and 16 and more room for wiring on the interior of element 13.

Mounted on circuit board 10 is high density chip carrier 30. On its lower surface 32, chip carrier 30 defines a high density array of electrical contact pads 34 arranged within a grid 44 defined by electrical contact pads 34 in the aggregate (see Figs. 3, 4 and 5). Solder balls 35 connect pads 34 to pads 20. Contact pads 34 are closely packed together in an array and arranged, in the particular embodiment shown, in columns 36 and rows 38 perpendicular thereto (Fig. 3). The contact pads 34 are in the same array as contacts 20 on surface 15 of the substrate.

As further illustrated in Fig. 3, electrical contact pads 34 are arranged in two groups, group A and group B. In particular, electrical contact pads 34 are arranged such that adjacent contact pads in each column, and adjacent contact pads in each row, are in different groups. This is shown in Fig. 3, where it can be seen that the two electrical contact pads 34 which are immediately adjacent "B" electrical contact pad 34 in column 40 are in group A, while the two electrical contact pads 34 which are immediately adjacent "B" electrical contact pads 34 in row 42 are also in group A. The pads of both group A and group B can be connected to surface 17 with blind vias.

In accordance with the present embodiment, through or primary holes 22 are arranged in an interstitial pattern or array corresponding to the array 32 of electrical contact pads 34 in chip carrier 30. By "interstitial array" is meant that the items in the array are arranged in rows and columns such that the items in one column are offset from the items in adjacent columns by approximately one half the distance between the items in the column. By "corresponding to array 32" is meant that primary through holes 22 align or register with selected electrical contact pads 34 in chip carrier 30 -- specifically, with "B" electrical contact pads 34 of the chip carrier in the particular embodiment shown.

This is illustrated in Fig. 4 which shows the pattern of primary through holes 22 in circuit board 10 as observed in the middle layer 13. As can be seen from this figure, each of primary through holes 22 is arranged in a column and a row in the same way as electrical contact pads 34 in chip carrier 30. In addition, primary through holes 22 are arranged so as to register with corresponding electrical contact pads 34 in the chip carrier. However, since primary through holes 22 are offset from one another so as to form a corresponding interstitial array, the number of primary through holes 22 is approximately one-half the number of electrical contact pads 34 in the chip carrier. Thus, primary through holes 22 register only with every other electrical contact pad 34 in chip carrier 30 in particular, only with "B" electrical contact pads 34 in chip carrier 30 in the embodiment shown.

With this arrangement, approximately one half of electrical contact pads 34 of chip carrier 30, i.e. all of the "B" contact pads, are electrically connected to primary holes 22 of the circuit board which are directly beneath the B contact pads 34. These holes 22 are contained within grid 44 which is the outer boundary of the connection pads 34 on the chip carrier 30. This leaves approximately half of the remaining electrical contacts of chip carrier 30, i.e. all of the "A" electrical contacts, remaining for electrical connection in another manner. (It is to be understood that more or less than half can be connected to holes 22, but one-half is a typical configuration.)

In accordance with the present embodiment, these "A" electrical contacts are connected by blind vias 21 to wiring lines or traces 24 and/or multiple additional or second wiring layers not shown on surfaces 15, 16, 17 and 18 to the secondary through holes 26 which are located outside the grid 44. This is illustrated in Figure 5, which shows that the plated through holes 26 are located outside the interstitial pattern in the grid 44. This can be accomplished in accordance with the present invention by any conventional means. For example, the surface mount technology (SMT) techniques and the blind via techniques described in U.S. Patent No. 5,424,492, U.S. Patent No. 5,451,721 and U.S. Patent No. 5,487,218 can be used for this purpose. The disclosures of these patents are incorporated herein by reference.

Many approaches have been taken in the past for maximizing wiring density. When through holes such as primary through holes 22 become too closely packed, the maximum number and line width of the traces that can be accommodated between adjacent holes become significantly reduced, especially in intermediate planes as well as the lower surface of the circuit board. This is a particular problem where the circuit board is designed so that most if not all of the through vias in the board are formed or "dropped" within the grid of the chip carrier. Arranging some of the through holes in an interstitial array within the grid and others outside it, as described above, greatly lessens this problem as considerably more space is provided between adjacent through holes.

It will therefore be appreciated that arrangement of through holes 26 outside the interstitial array of primary through holes 22 allows sufficient expansion of the spaces between all adjacent through holes in the device. At the same time, it also keeps the device geometry, as a whole, as compact as possible. As a result, the desired goals of higher flexibility and greater density in component wiring is achieved without unduly increasing the overall size of the device. This is of particular advantage in modern electronic components where miniaturization is a continual goal.

In summary, there is described a circuit board is provided which has contacts on the surface arrayed to engage contact pads on a chip carrier bounded by a grid. A plurality of primary through holes are provided in the circuit board location within the grid and electrically connected to chip contact pads thereabove. A plurality of secondary through holes are provided which are located outside the grid and electrically connected to the inside of the chip contact pads.

Although only a few embodiments of the present invention have been described above, it should be appreciated that many modifications can be made without departing from the spirit and scope of the invention. For example, although the foregoing description has illustrated the interstitial arrays of Figs. 3 and 4 as being composed of orthagonally-arranged rows and columns, it should be appreciated that an interstitial array can be composed of rows and columns arranged at an acute angle with respect to one another or even arranged in a circle. In addition, it should be appreciated that the holes 26 also can be filled plated-through-hole as are holes 22. All such modifications are intended to be included within the scope of the present invention, which is to be limited only by the following claims:

Claims

1. A multi-layer circuit board for receiving a chip carrier having a high density array of electrical contact pads arranged in a grid, said circuit board comprising

   an electrically insulating substrate having upper and lower surfaces,
   a plurality of electrical contacts on said upper surface for connection to the electrical contact pads of said chip carrier,
   a first wiring layer having electrical contacts therein,
   a second wiring layer having wiring traces therein, said second wiring layer being associated with the upper surface of said substrate,
   wherein said circuit board has primary through holes arranged within said grid in an interstitial array and secondary through holes located outside said grid, said primary through holes being in electrical communication with respective first electrical contacts of said upper surface,
   respective second electrical contacts on said upper surfaces being in electrical contact with said second through holes.

2. A circuit board as claimed in claim 1, wherein the electrical contacts in said mounting pad are arranged in columns and rows, the electrical contacts in each column being aligned with the electrical contacts in adjacent rows, said electrical contacts being arranged in groups of first electrical contacts and second electrical contacts such that the contact pads immediately adjacent each contact pad are in a different group from that contact pad.

3. A circuit board as claimed in claim 2, wherein said columns and rows are arranged at right angle to one another.

4. A circuit board as claimed in claim 1, 2, or 3 wherein said primary through holes are filled.

5. A circuit board as claimed in any of the preceding claims further characterized by blind vias interconnecting the first wiring layer to the second wiring layer.

6. A circuit board of claim 5 wherein said second wiring layer is carried on the upper surface of said substrate.

7. A circuit board as claimed in any of claims 1 to 4 wherein said first wiring layer is on the lower surface of said substrate.

8. A circuit board of claim 7, wherein said second wiring layer is intermediate the upper and lower surfaces of said substrate, and further wherein the second electrical contacts of said mounting pad are electrically connected to respective wiring traces of said second wiring layer by means of blind vias.

9. A circuit board of claim 8 wherein said circuit board includes multiple second wiring layers intermediate said upper and lower surfaces, at least one second electrical contact being in electrical contact with each of said second wiring layers.

10. A circuit board as claimed in any of the preceding claims wherein said circuit board defines secondary through vias arranged outside said grid, said secondary through vias also being in electrical communication with respective first electrical contacts of said mounting pad and also with respective wiring traces of said first wiring layer.

11. The circuit board of claim 10 wherein said secondary through vias are arranged in the same interstitial array as said primary through vias.

12. A method of forming a multilayer circuit board for receiving a chip carrier having a high density array of electrical contact pads arrayed in a grid comprising the steps of;

    providing an electrically insulating substrate having upper and lower surfaces,
    forming a plurality of electrical contacts on said

upper surface for connecting to the electrical contact pads of said chip carrier,
forming a first wiring layer having electrical contacts therein,
forming a second wiring layer having wiring traces therein associated with said upper surface of said substrate,
forming a plurality of primary through holes within said grid in an interstitial array and a plurality of secondary through holes located outside said grid,
electrically connecting said primary through holes with first electrical contacts on said upper surface, and electrically connecting second electrical contacts on said upper surface with said secondary through holes.

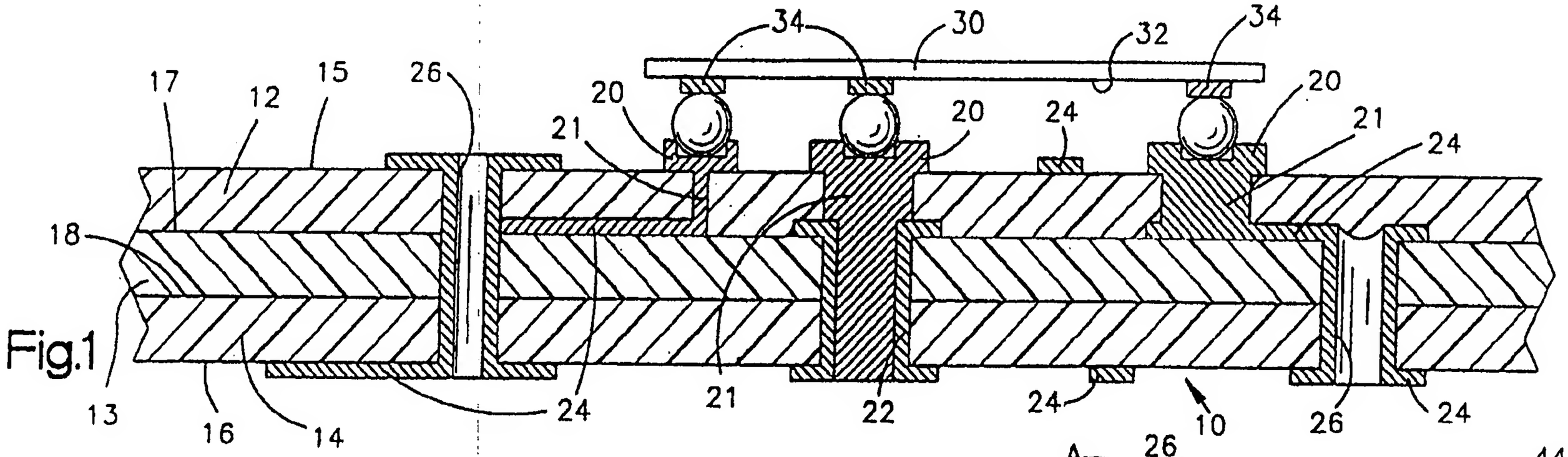

Fig.1

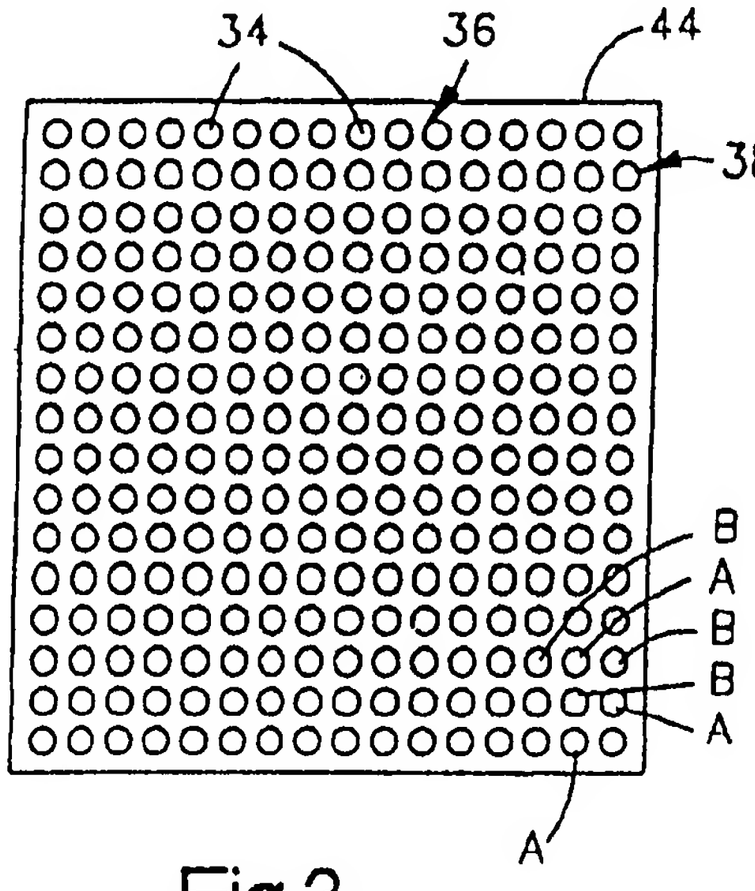

Fig.3

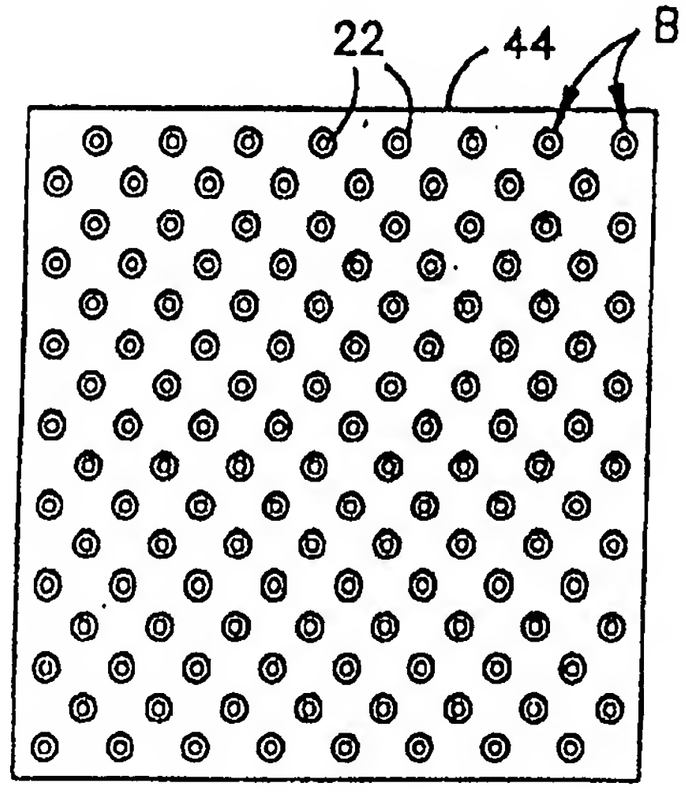

Fig.4

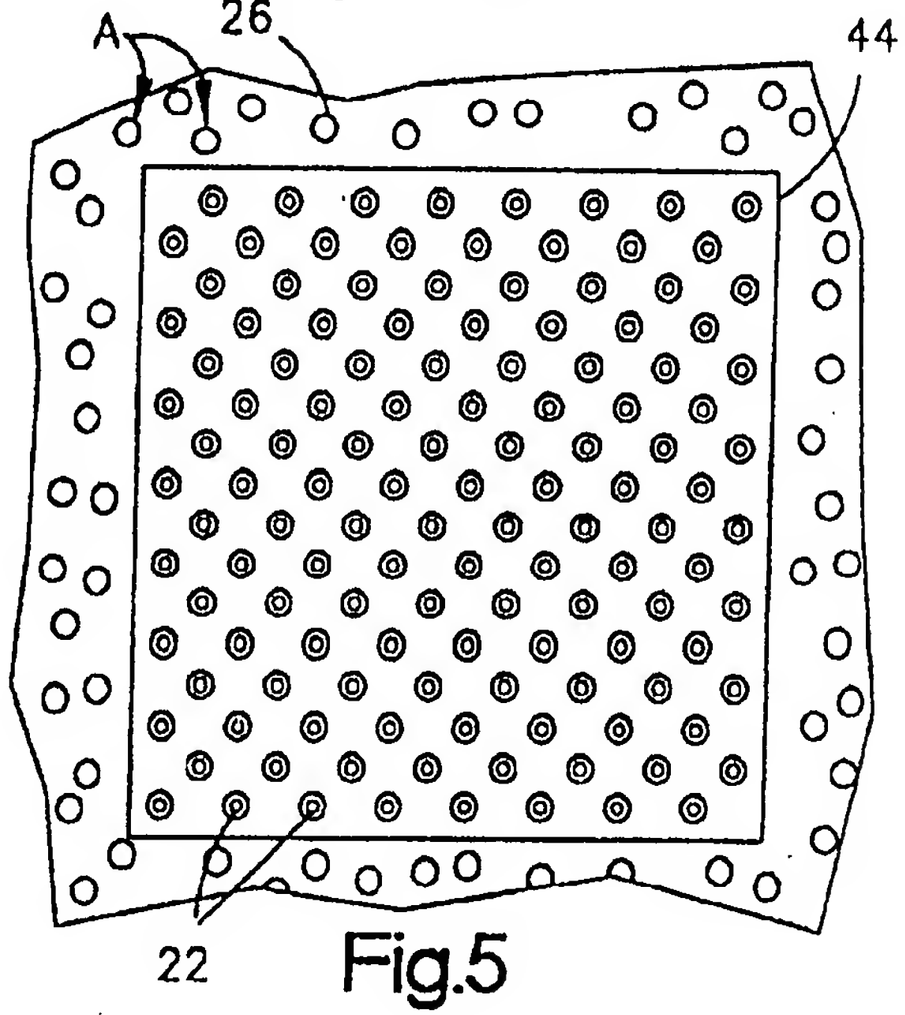

Fig.5

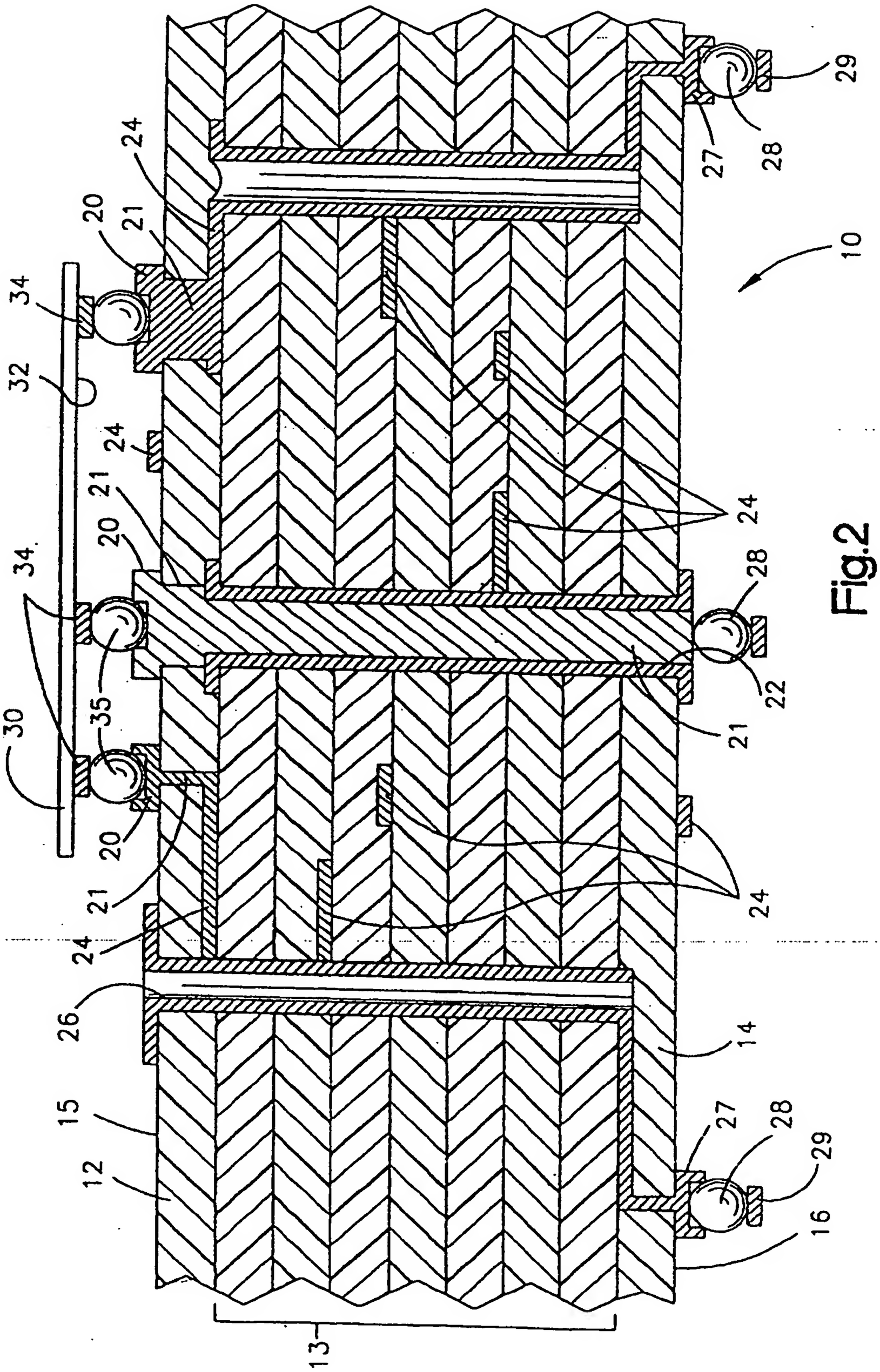

Fig.2

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 98 30 4126

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
A	US 4 598 167 A (USHIFUSA NOBUYUKI ET AL) 1 July 1986 * the whole document *	1-12	H05K3/40 H05K1/00 H01L23/498
A	EP 0 660 405 A (IBM) 28 June 1995 * the whole document *	1-12	
A	WO 94 18701 A (GORE & ASS) 18 August 1994 * the whole document *	1-12	
A	WO 96 08037 A (SHELDAHL INC) 14 March 1996 * the whole document *	1-12	
			TECHNICAL FIELDS SEARCHED (Int.Cl.6) H05K H01L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
MUNICH	14 September 1998	Torti, C

CATEGORY OF CITED DOCUMENTS

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